

General Description

The MAX13450E/MAX13451E are half-duplex and fullduplex RS-485/RS-422 transceivers. These devices feature internal 100Ω and 120Ω termination resistors. The resistor values are pin selectable. A logic supply input allows interfacing to logic levels down to +1.8V.

The MAX13450E/MAX13451E feature strong drivers specified to drive low-impedance lines found when a fully loaded bus, based on today's 100Ω characteristic impedance cable, is doubly terminated. Both devices allow slew-rate limiting of the driver output to reduce EMI and reflections for data rates up to 500kbps.

The MAX13451E has a FAULT alarm indication output to signal to the system that an error condition exists in the driver. The MAX13451E also features a logic inversion function. The logic inversion allows phase reversal of the A-B signals in case these are inadvertently connected wrongly.

The MAX13450E/MAX13451E have 1/8-unit load receiver input impedance, allowing up to 256 transceivers on the bus. All driver outputs are protected to ±30kV ESD using the Human Body Model (HBM).

The MAX13450E/MAX13451E are available in a 14-pin TSSOP package and operate over the automotive -40°C to +125°C temperature range.

Applications

Industrial Control Systems Portable Industrial Equipment Motor Control Security Networks

Medical Networks

Ordering Information/ **Selector Guide**

| PART | HALF/FULL DUPLEX | PIN-PACKAGE | |
|---------------|---------------------|--------------|--|
| MAX13450EAUD+ | Full | 14 TSSOP-EP* | |
| MAX13451EAUD+ | Half | 14 TSSOP-EP* | |

Note: All devices are specified over the -40°C to +125°C operating temperature range.

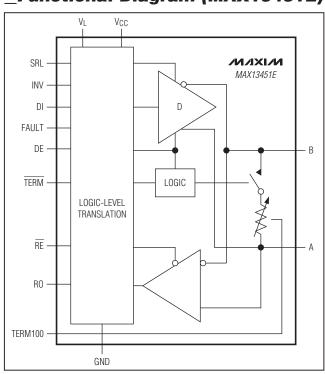
+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Features

- ♦ 100Ω/120Ω Pin-Selectable Internal Termination Resistors
- ♦ Driver Drives 100Ω Double Termination
- ♦ 20Mbps (max) Data Rate
- ♦ Pin-Selectable Slew-Rate Limiting
- ♦ Logic Supply Input Allows Interfacing Down to 1.8V
- ◆ Driver Fault-Indication Output (MAX13451E)
- ◆ Inverting of A, B Line Polarity (MAX13451E)
- ♦ High-Impedance Driver Output/Receiver Input When Vcc Supply is Removed
- ♦ Hot-Swap Input Structure on DE, RE, and TERM
- ♦ Extended ESD Protection ±30kV Human Body Model ±15kV Air Gap Discharge per IEC 61000-4-2 ±7kV Contact Discharge per IEC 61000-4-2
- ♦ 1/8-Unit Load Allows Up to 256 Transceivers on the Bus
- Thermal and Overcurrent Protected
- ♦ Fail-Safe Receivers
- ♦ +4.5V to +5.5V Supply Voltage Range

Functional Diagram (MAX13451E)



/U/IXI/U

Maxim Integrated Products 1

ABSOLUTE MAXIMUM RATINGS

| (All voltages referenced to GND.) |
|---|
| VCC, VL0.3V to +6V |
| DE, RE, DI, RO, TERM, TERM100, SRL0.3V to (VL + 0.3V) |
| INV, FAULT0.3V to (V _L + 0.3V) |
| A, B, Z, Y8V to +13V |
| A to B (High-Z State)+14V |
| B to A (High-Z State)+14V |
| Short-Circuit Duration (RO, Y, Z) to GND Continuous |
| Continuous Power Dissipation ($T_A = +70^{\circ}C$) |
| 14-Pin TSSOP (derate 25.6mW/°C above +70°C)2051mW |

| Package Junction-to-Ambient Thermal Resistance (θJA) (Note 1) | 39°C/W |
|---|----------------|
| Package Junction-to-Case Thermal | , |
| Resistance (θJC) (Note 1) | 3°C/W |
| Operating Temperature Range | 40°C to +125°C |
| Storage Temperature Range | 65°C to +150°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | |
| Soldering Temperature (reflow) | +260°C |

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCC = +4.5V to +5.5V, V_L = +1.62V to 4.2V, T_A = T_{MIN} to T_{MAX} , unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +1.8V, and T_A = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|------------------|---|------|--------------------|------|-------|--|
| Supply Voltage | Vcc | | 4.5 | | 5.5 | V | |
| Logic Supply Voltage | VL | | 1.62 | 1.8 | 4.2 | V | |
| Cupply Current | loo | $DE = \overline{RE} = high, \overline{TERM} = high, no load$ | | | 6 | mA | |
| Supply Current | Icc | $\overline{DE} = \overline{RE} = low, \overline{TERM} = low, no load$ | | | 12 | IIIA | |
| Logic Supply Current | ΙL | Current into V_L , no load on RO, device not switching, $DE = \overline{RE} = high$ | | | 2 | μA | |
| Shutdown Current | ISHDN | Current into V_{CC} , $DE = low$, $\overline{RE} = \overline{TERM} = high$ | | | 30 | μA | |
| Shutdown Current | ISHDIN | Current into V_{CC} , DE = low, \overline{RE} = high, \overline{TERM} = low | | | 8 | mA | |
| DRIVER | | | | | | | |
| Differential Driver Output | Vod | RDIFF = 100Ω , Figure 1 (Note 3) | 2.0 | | Vcc | - V | |
| Differential Driver Output | | $R_{DIFF} = 46\Omega$, Figure 1 (Note 3) | 1.5 | | Vcc | | |
| Change in Magnitude of Differential Output Voltage | ΔV _{OD} | R_{DIFF} = 100 Ω or 46 Ω , Figure 1 (Note 3) | | | 0.2 | V | |
| Driver Common-Mode Output Voltage | Voc | R_{DIFF} = 100 Ω or 46 Ω , Figure 1 (Note 3) | | V _{CC} /2 | 3 | V | |
| Change In Magnitude of Common-Mode Voltage | ΔV _{OC} | R_{DIFF} = 100 Ω or 46 Ω , Figure 1 (Note 3) | | | 0.2 | V | |
| river Short-Circuit Output | | $0V \le V_{OUT} \le +12V$ | | | +280 | m A | |
| Current | losp | -7V ≤ V _{OUT} ≤ 0V | -250 | | | mA mA | |
| Driver Short-Circuit Foldback | IOSDF | $(V_{CC} - 1V) \le V_{OUT} \le +12V$ | +15 | | | mA | |
| Output Current | 10201 | -7V ≤ V _{OUT} ≤ 0V | | | -15 | 111/ | |

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{CC} = +4.5V \text{ to } +5.5V, V_L = +1.62V \text{ to } 4.2V, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted.}$ Typical values are at $V_{CC} = +5V, V_L = +1.8V, \text{ and } T_A = +25^{\circ}C.)$ (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|------------------|---|-----------------------|----------------------|-------|----------------------|-------|
| RECEIVER | • | | | | | | |
| Input Current (A and B) | IA, B | DE = RE = GND; TERM = VL; VCC = GND | VA or VB = +12V | | | 125 | μA |
| Input Guirent (A and B) | IA, B | or 5.5V | VA or VB = -7V | -100 | | | μΑ |
| Receiver Differential Threshold Voltage | V _{TH} | $ \begin{array}{l} -7V \leq V_{CM} \leq +12V, \\ DE = \overline{RE} = GND; \\ \overline{TERM} = V_{L}; V_{CC} = GND \end{array} $ | V_A or $V_B = +12V$ | -200 | | -50 | mV |
| Receiver Input Hysteresis | ΔVTH | VA + VB = 0V | | | 15 | | mV |
| LOGIC INTERFACE | | | | | | | |
| Input High Voltage | VIH | DI, DE, RE, TERM, SRL, T | ERM100, INV | 2/3 x VL | | | V |
| Input Low Voltage | VIL | DI, DE, RE, TERM, SRL, T | ERM100, INV | | | 1/3 x V _L | V |
| Input Current | IIN | DI, DE, RE, TERM, TERM | 100, SRL, INV | -1 | | +1 | μΑ |
| Receiver Output High Voltage | VROH | I _{OUT} = -1mA | | V _L - 0.6 | | | V |
| Receiver Output Low Voltage | VROL | IOUT = +1mA | | | | 0.4 | V |
| Three-State Output Current at Receiver | lozr | 0V ≤ VRO ≤ VL | | -1 | +0.01 | +1 | μΑ |
| Receiver Output Short-Circuit Current | IOSR | $0V \le V_{RO} \le V_L$ | | ±1 | | ±80 | mA |
| Fault Output High Voltage (MAX13451E) | VFAULTH | Fault condition, IOUT = -1 | mA | VL - 0.6 | | | V |
| Fault Output Low Voltage (MAX13451E) | VFAULTL | Nonfault condition; IOUT = | = +1mA | | | 0.4 | V |
| TERMINATION RESISTOR | | | | | | | |
| 100Ω Termination Resistor | R ₁₀₀ | TERM = low, TERM100 = | high | 85 | 100 | 115 | Ω |
| 120Ω Termination Resistor | R ₁₂₀ | TERM = low, TERM100 = | low | 101 | 120 | 139 | Ω |
| Single-Ended Input Capacitance vs. GND | CIN | f = 1MHz (MAX13451E only) | | | 40 | | рF |
| ESD PROTECTION | | | | | | | |
| | | Human Body Model | | | ±30 | | |
| ESD Protection (A, B, Y, Z) | | IEC 61000-4-2 Air Gap Di | ischarge | | ±15 | | kV |
| • | | IEC 61000-4-2 Contact Di | ischarge | | ±7 | | |
| ESD Protection (All Other Pins) | | Human Body Model | | | ±2 | | |

SWITCHING CHARACTERISTICS—SRL = HIGH

(VCC = +4.5V to +5.5V, V_L = +1.62V to 4.2V, T_A = T_{MIN} to T_{MAX} , unless otherwise noted. Typical values are at VCC = +5V, V_L = +1.8V and T_A = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | TYP | MAX | UNITS |
|---|------------------------|---|-----|-----|----------|-------|
| DRIVER | , | | | | | |
| Driver Propagation Delay | tDPLH | Douge 540 Ct. 50nE Figures 2 and 2 | | | 800 | 20 |
| Driver Propagation Delay | tDPHL | RDIFF = 54Ω , CL = 50pF, Figures 2 and 3 | | | 800 | ns |
| Differential Driver Output Skew ItDPLH - tDPHLI | tDSKEW | RDIFF = 54Ω , CL = 50pF, Figure 3 | | | 100 | ns |
| Driver Differential Output Rise or | tHL | Douge 540 Ct. FORE Figures 2 and 2 | 100 | | 600 | |
| Fall Time | tLH | RDIFF = 54Ω , C _L = 50 pF, Figures 2 and 3 | 100 | | 600 | ns |
| Maximum Data Rate | DR _{MAX} | | 500 | | | kbps |
| Driver Enable from Shutdown to Output High | tDZH(SHDN) | S2 closed, $R_L = 500\Omega$, $C_L = 100pF$, Figures 4 and 5 | | | 4500 | ns |
| Driver Enable from Shutdown to Output Low | tDZL(SHDN) | S1 closed, $R_L = 500\Omega$, $C_L = 100pF$, Figures 4 and 5 | | | 5200 | ns |
| Driver Disable Delay | tDLZ, tDHZ | Figures 4 and 5 | | | 100 | ns |
| Driver Enable Delay | tdzl, tdzh | Figures 4 and 5 | | | 2500 | ns |
| RECEIVER | | | | | | |
| Receiver Propagation Delay | trplh | $C_L = 15pF$, $ V_{ID} \ge 2.0V$; t_{LH} , $t_{HL} \le 15ns$, | | | 200 | ns |
| Theceiver i Topagation Delay | trphl | Figures 6 and 7 | | | 200 | 115 |
| Receiver Output Skew | trskew | C _L = 15pF, Figures 6 and 7 | | | 30 | ns |
| Maximum Data Rate | DR _{MAX} | | 500 | | | kbps |
| Receiver Enable to Output High | [†] RZH | S2 closed, C_L = 100pF, R_L = 500 Ω , Figures 8 and 9 | | | 50 | ns |
| Receiver Enable to Output Low | tRZL | S1 closed, C_L = 100pF, R_L = 500 Ω , Figures 8 and 9 | | | 50 | ns |
| Receiver Disable from High | tRHZ | Figures 8 and 9 | | | 50 | ns |
| Receiver Disable from Low | tRLZ | Figures 8 and 9 | | | 50 | ns |
| Receiver Enable from Shutdown to Output High | tRZH(SHDN) | Figures 8 and 9 | | | 5000 | ns |
| Receiver Enable from Shutdown to Output Low | [†] RZL(SHDN) | Figures 8 and 9 | | | 5000 | ns |
| TERMINATION RESISTOR | | | | | | |
| Turn-Off Time | trtz | Figure 10 | | 120 | | μs |
| Turn-On Time | trten | Figure 10 | | 1 | <u> </u> | μs |

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SWITCHING CHARACTERISTICS—SRL = LOW

(VCC = +4.5V to +5.5V, V_L = +1.62V to 4.2V, T_A = T_{MIN} to T_{MAX} , unless otherwise noted. Typical values are at V_{CC} = +5V, V_L = +1.8V, and T_A = +25°C.) (Note 2)

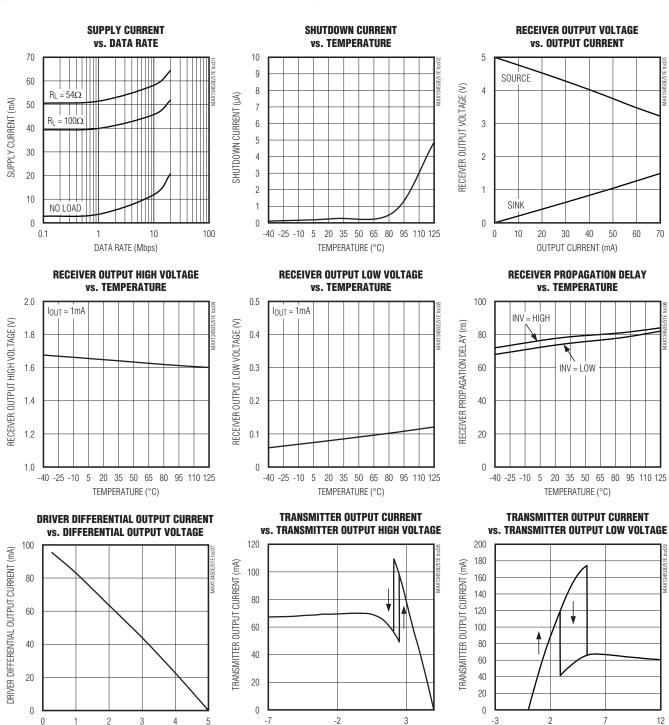
| DRIVER Topy Top | PARAMETER | PARAMETER SYMBOL CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---------------------------------|-----------------------------|---|-----|-----|------|-------|
| Driver Propagation Delay TOPHIL | DRIVER | , | | | | | |
| TOPHIL | Driver Propagation Delay | tDPLH | Pour 540 Ct 50nE Figures 2 and 2 | | | 50 | no |
| ItDPLH - TDPHLI | Driver Fropagation Delay | tDPHL | $\frac{1}{1}$ NDIFF = 5412, OL = 50pF, Figures 2 and 5 | | | 50 | 115 |
| Fall Time THL, tLH HDIFF = 34Ω, CL = SUPF, Figures 2 and 3 15 ns | · · | tDSKEW | RDIFF = 54Ω , CL = 50pF, Figure 3 | | | 6 | ns |
| Driver Enable from Shutdown to Output High 0 to ZH(SHDN) Figures 4 and 5 0 to ZH(SHDN) Figures 4 and 5 0 to ZH(SHDN) S1 closed, RL = 500Ω, CL = 100pF, Figures 4 and 5 0 to ZH(SHDN) Prigores 4 and 5 0 to ZH(SHDN) S1 closed, RL = 500Ω, CL = 100pF, Figures 4 and 5 0 to ZH(SHDN) Prigores 6 and 5 0 to ZH(SHDN) Prigores 6 and 7 0 to ZH(SHDN) Prigores 6 and 7 0 to ZH(SHDN) Prigores 6 and 7 0 to ZH(SHDN) Prigores 8 and 9 0 to ZH(ZH(SHDN)) Prigores 8 and 9 0 to ZH(ZH(S | | tHL, tLH | RDIFF = 54Ω , CL = 50pF, Figures 2 and 3 | | | 15 | ns |
| Output High IDZH(SHDN) Figures 4 and 5 2000 ns Driver Enable from Shutdown to Output Low tDZL(SHDN) \$1 closed, RL = 500Ω, CL = 100pF, Figures 4 and 5 2000 ns Driver Disable Delay tDZL, tDZL Figures 4 and 5 100 ns Driver Enable Delay tDZL, tDZH Figures 4 and 5 100 ns RECEIVER *** TapLH*** TapLH**** TapLH*** TapLH**** TapLH**** TapLH**** TapLH**** TapLH**** TapLH***** TapLH**** TapLH**** TapLH***** TapLH***** TapLH***** TapLH******* TapLH***** TapLH***** TapLH************************************ | Maximum Data Rate | DRMAX | | 20 | | | Mbps |
| Output Low IDZL(SHDN) Figures 4 and 5 2000 fis Driver Disable Delay tDLZ, tDHZ Figures 4 and 5 100 ns Driver Enable Delay tDZL, tDZH Figures 4 and 5 100 ns RECEIVER Receiver Propagation Delay tRPLH tRPHL CL = 15pF, IVIDI ≥ 2.0V; tLH, tHL ≤ 15ns, Figures 6 and 7 50 ns Receiver Output Skew tRSKEW CL = 15pF, Figures 6 and 7 6 ns Maximum Data Rate DRMAX 20 Mbps Receiver Enable to Output High tRZH S2 closed, CL = 100pF, RL = 500Ω, Figures 8 and 9 50 ns Receiver Enable to Output Low tRZL Figures 8 and 9 50 ns Receiver Disable Time from High tRHZ Figures 8 and 9 50 ns Receiver Enable from Shutdown to Output High tRZH(SHDN) Figures 8 and 9 50 ns Receiver Enable from Shutdown to Output Low tRZH(SHDN) Figures 8 and 9 2000 ns Receiver Enable from Shutdown to Output Low tRZH(SHDN) Figures 8 and 9 <td< td=""><td></td><td>tDZH(SHDN)</td><td>I to the second second</td><td></td><td></td><td>2000</td><td>ns</td></td<> | | tDZH(SHDN) | I to the second | | | 2000 | ns |
| Driver Enable Delay tDZL, tDZH Figures 4 and 5 100 ns RECEIVER Receiver Propagation Delay tRPLH tRPHL CL = 15pF, IVIpI ≥ 2.0V; tLH, tHL ≤ 15ns, Figures 6 and 7 50 ns Receiver Output Skew tRSKEW CL = 15pF, Figures 6 and 7 6 ns Maximum Data Rate DRMAX 20 Mbps Receiver Enable to Output High tRZH S2 closed, CL = 100pF, RL = 500Ω, Figures 8 and 9 50 ns Receiver Enable to Output Low tRZL S1 closed, CL = 100pF, RL = 500Ω, Figures 8 and 9 50 ns Receiver Disable Time from High Receiver Disable Time from Low tRLZ Figures 8 and 9 50 ns Receiver Enable from Shutdown to Output High tRZH(SHDN) Figures 8 and 9 50 ns Receiver Enable from Shutdown to Output Low tRZL(SHDN) Figures 8 and 9 2000 ns TERMINATION RESISTOR Turn-Off Time tRTZ Figure 10 120 μs | | tDZL(SHDN) | | | | 2000 | ns |
| RECEIVERReceiver Propagation Delay $tRPLH$ tRP | Driver Disable Delay | tDLZ, tDHZ | Figures 4 and 5 | | | 100 | ns |
| Receiver Propagation DelaytRPLH tRPHLCL = 15pF, IVIDI ≥ 2.0V; tLH, tHL ≤ 15ns, Figures 6 and 750nsReceiver Output SkewtRSKEWCL = 15pF, Figures 6 and 76nsMaximum Data RateDRMAX20MbpsReceiver Enable to Output HightRZHS2 closed, CL = 100pF, RL = 500Ω, Figures 8 and 950nsReceiver Enable to Output LowtRZLS1 closed, CL = 100pF, RL = 500Ω, Figures 8 and 950nsReceiver Disable Time from High Receiver Disable Time from LowtRHZFigures 8 and 950nsReceiver Enable from Shutdown to Output HightRZH(SHDN)Figures 8 and 950nsReceiver Enable from Shutdown to Output LowtRZL(SHDN)Figures 8 and 92000nsTERMINATION RESISTORtRTZFigure 10120μs | Driver Enable Delay | tdzl, tdzh | Figures 4 and 5 | | | 100 | ns |
| Receiver Propagation DelaytRPHLFigures 6 and 750Receiver Output SkewtRSKEWCL = 15pF, Figures 6 and 76nsMaximum Data RateDRMAX20MbpsReceiver Enable to Output HightRZH\$2 closed, CL = 100pF, RL = 500Ω, Figures 8 and 950nsReceiver Enable to Output LowtRZL\$1 closed, CL = 100pF, RL = 500Ω, Figures 8 and 950nsReceiver Disable Time from HightRHZFigures 8 and 950nsReceiver Disable Time from LowtRLZFigures 8 and 950nsReceiver Enable from Shutdown to Output HightRZH(SHDN)Figures 8 and 92000nsReceiver Enable from Shutdown to Output LowtRZL(SHDN)Figures 8 and 92000nsTERMINATION RESISTORTurn-Off TimetRTZFigure 10120μs | RECEIVER | | | | | | |
| tRPHLFigures 6 and 7Receiver Output SkewtRSKEWCL = 15pF, Figures 6 and 76nsMaximum Data RateDRMAX20MbpsReceiver Enable to Output HightRZH\$2 closed, CL = 100pF, RL = 500Ω, Figures 8 and 950nsReceiver Enable to Output LowtRZL\$1 closed, CL = 100pF, RL = 500Ω, Figures 8 and 950nsReceiver Disable Time from HightRHZFigures 8 and 950nsReceiver Disable Time from LowtRLZFigures 8 and 950nsReceiver Enable from Shutdown to Output HightRZH(SHDN)Figures 8 and 92000nsReceiver Enable from Shutdown to Output LowtRZL(SHDN)Figures 8 and 92000nsTERMINATION RESISTORTurn-Off TimetRTZFigure 10120μs | Pacaivar Propagation Dalay | trplh | \Box C _L = 15pF, \Box \Box \Box 2.0V; \Box \Box \Box \Box 15ns, | | | 50 | ne |
| Maximum Data RateDRMAX20MbpsReceiver Enable to Output HightRZHS2 closed, CL = 100pF, RL = 500Ω, Figures 8 and 950nsReceiver Enable to Output LowtRZLS1 closed, CL = 100pF, RL = 500Ω, Figures 8 and 950nsReceiver Disable Time from HightRHZFigures 8 and 950nsReceiver Disable Time from LowtRLZFigures 8 and 950nsReceiver Enable from Shutdown to Output HightRZH(SHDN)Figures 8 and 92000nsReceiver Enable from Shutdown to Output LowtRZL(SHDN)Figures 8 and 92000nsTERMINATION RESISTORtRTZFigure 10120μs | Theceiver i Topagation Delay | trphl | Figures 6 and 7 | | | 50 | 115 |
| Receiver Enable to Output HightRZHS2 closed, CL = 100pF, RL = 500Ω, Figures 8 and 950nsReceiver Enable to Output LowtRZLS1 closed, CL = 100pF, RL = 500Ω, Figures 8 and 950nsReceiver Disable Time from HightRHZFigures 8 and 950nsReceiver Disable Time from LowtRLZFigures 8 and 950nsReceiver Enable from Shutdown to Output HightRZH(SHDN)Figures 8 and 92000nsReceiver Enable from Shutdown to Output LowtRZL(SHDN)Figures 8 and 92000nsTERMINATION RESISTORTurn-Off TimetRTZFigure 10120μs | Receiver Output Skew | trskew | C _L = 15pF, Figures 6 and 7 | | | 6 | ns |
| Receiver Enable to Output High tRZH Figures 8 and 9 50 ns Receiver Enable to Output Low tRZL S1 closed, CL = 100pF, RL = 500Ω, Figures 8 and 9 50 ns Receiver Disable Time from High tRHZ Figures 8 and 9 50 ns Receiver Disable Time from Low tRLZ Figures 8 and 9 50 ns Receiver Enable from Shutdown to Output High tRZH(SHDN) Figures 8 and 9 2000 ns Receiver Enable from Shutdown to Output Low tRZL(SHDN) Figures 8 and 9 2000 ns TERMINATION RESISTOR Turn-Off Time tRTZ Figure 10 120 μs | Maximum Data Rate | DRMAX | | 20 | | | Mbps |
| Receiver Enable to Output Low | Receiver Enable to Output High | tRZH | | | | 50 | ns |
| Receiver Disable Time from Low transcript Figures 8 and 9 50 ns Receiver Enable from Shutdown to Output High transcript Figures 8 and 9 2000 ns Receiver Enable from Shutdown to Output Low transcript Figures 8 and 9 2000 ns TERMINATION RESISTOR Turn-Off Time transcript Figure 10 120 µs | Receiver Enable to Output Low | t _{RZL} | | | | 50 | ns |
| Receiver Enable from Shutdown to Output High tRZH(SHDN) Figures 8 and 9 2000 ns Receiver Enable from Shutdown to Output Low tRZL(SHDN) Figures 8 and 9 2000 ns TERMINATION RESISTOR Turn-Off Time tRTZ Figure 10 120 μs | Receiver Disable Time from High | tRHZ | Figures 8 and 9 | | | 50 | ns |
| to Output High Receiver Enable from Shutdown to Output Low TERMINATION RESISTOR Turn-Off Time TRZH(SHDN) Figures 8 and 9 2000 ns 2000 ns | Receiver Disable Time from Low | tRLZ | Figures 8 and 9 | | | 50 | ns |
| to Output Low | | tRZH(SHDN) | Figures 8 and 9 | | | 2000 | ns |
| Turn-Off Time tRTZ Figure 10 120 μs | | tRZL(SHDN) | Figures 8 and 9 | | | 2000 | ns |
| | TERMINATION RESISTOR | • | | | | | |
| Turn-On Time t _{RTEN} Figure 10 1 μs | Turn-Off Time | trtz | Figure 10 | | 120 | | μs |
| | Turn-On Time | tRTEN | Figure 10 | | 1 | | μs |

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 3: Termination resistance is disabled (TERM = high).

Typical Operating Characteristics

 $(V_{CC} = +5V, V_L = +1.8V, T_A = +25^{\circ}C, unless otherwise noted.)$



TRANSMITTER OUTPUT HIGH VOLTAGE (V)

TRANSMITTER OUTPUT LOW VOLTAGE (V)

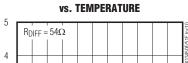
DRIVER DIFFERENTIAL OUTPUT VOLTAGE (V)

140

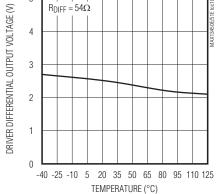
40 20

Typical Operating Characteristics (continued)

 $(V_{CC} = +5V, V_L = +1.8V, T_A = +25^{\circ}C, unless otherwise noted.)$



DRIVER DIFFERENTIAL OUTPUT VOLTAGE



120 100 MAGNITUDE (Ω) 80 R₁₀₀ MAGNITUDE 60 R₁₀₀ PHASE

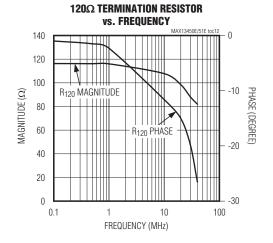
 100Ω TERMINATION RESISTOR

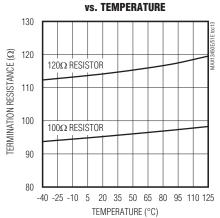
vs. FREQUENCY



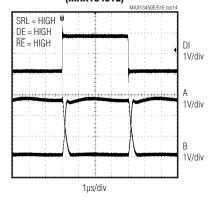
-30

100

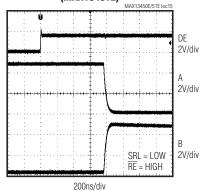




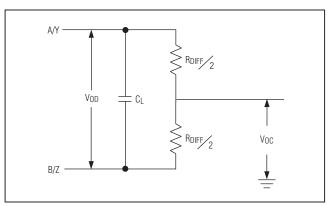
DRIVER PROPAGATION DELAY (250kbps) (MAX13451E)



DRIVER ENABLE TIME FROM SHUTDOWN (MAX13451E)



Test Circuits and Waveforms



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Figure 1. Driver DC Test Load

Figure 2. Driver Timing Test Circuit

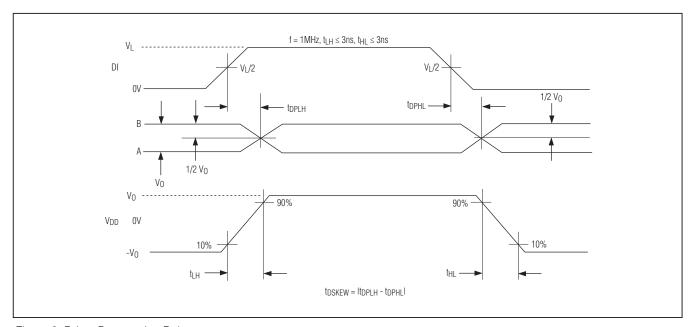


Figure 3. Driver Propagation Delays

Test Circuits and Waveforms (continued)

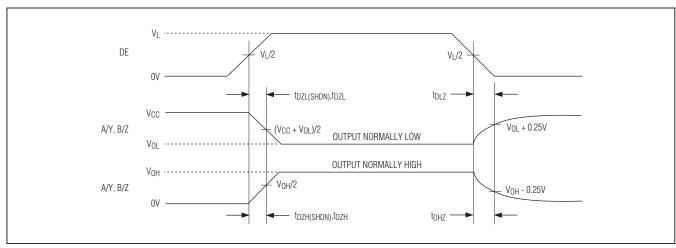


Figure 4. Driver Enable and Disable Times

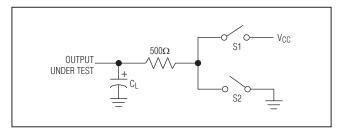


Figure 5. Driver-Enable and Disable-Timing Test Load

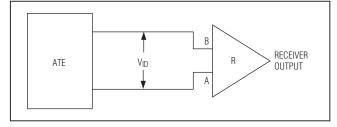


Figure 6. Receiver Propagation Delay Test Circuit

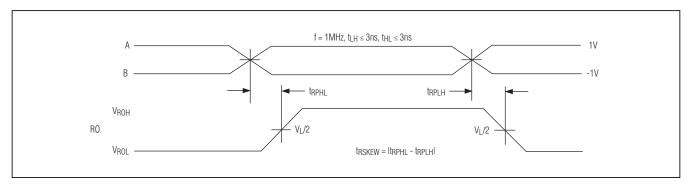


Figure 7. Receiver Propagation Delays

Test Circuits and Waveforms (continued)

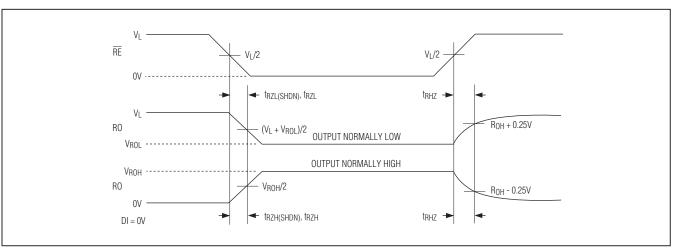


Figure 8. Receiver Enable and Disable Times

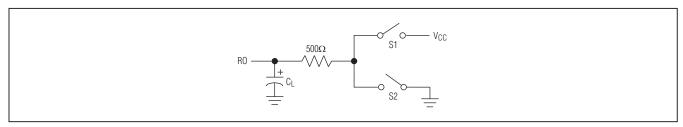


Figure 9. Receiver Enable and Disable Times

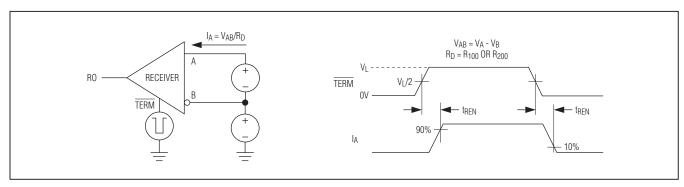
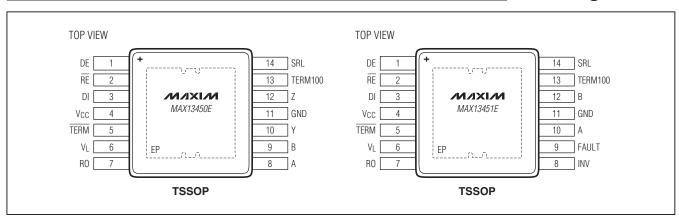


Figure 10. Termination Resistor Turn-On/-Off Times

Pin Configurations



Pin Description

| PIN | | NAME | FUNCTION |
|-----------|-----------|------|---|
| MAX13450E | MAX13451E | NAME | FUNCTION |
| 1 | 1 | DE | Driver-Output Enable. Drive DE low to put the driver output in three-state. Drive DE high to enable the driver. DE is referenced to V _L . |
| 2 | 2 | RE | Receiver-Output Enable. Drive \overline{RE} low to enable the RO. Drive \overline{RE} high to disable the RO output and put the RO output in a high-impedance state. \overline{RE} is referenced to VL. |
| 3 | 3 | DI | Driver Input. Drive DI low to force the noninverting output low and the inverting output high. Drive DI high to force the noninverting output high and inverting output low. DI is referenced to V _L . |
| 4 | 4 | Vcc | Power-Supply Voltage. Bypass V _{CC} to GND with a 0.1µF ceramic capacitor placed as close as possible to the device. |
| 5 | 5 | TERM | Active-Low Termination Resistor Enable. Drive $\overline{\text{TERM}}$ low to enable the internal termination resistor. $\overline{\text{TERM}}$ is referenced to V_L . |
| 6 | 6 | VL | Logic Supply Voltage. Bypass V _L to GND with a 0.1µF ceramic capacitor placed as close as possible to the device. |
| 7 | _ | RO | Receiver Output. When receiver is enabled and V_A - $V_B \ge$ -50mV, RO is high. If V_A - $V_B \le$ -200mV, RO is low. RO is referenced to V_L . |
| _ | 7 | RO | Receiver Output. When INV is low, receiver is enabled and V_A - $V_B \ge$ -50mV, RO is high. If V_A - $V_B \le$ -200mV, RO is low. When INV is high, receiver is enabled and V_A - $V_B \ge$ -50mV, RO is low. If V_A - $V_B \le$ -200mV, RO is high. RO is referenced to V_L . |
| 8 | _ | А | Noninverting Receiver Input |
| _ | 10 | А | If INV is low, A is a noninverting receiver input and a noninverting driver output. If INV is high, A is an inverting receiver input and an inverting driver output. |
| 9 | _ | В | Inverting Receiver Input |
| _ | 12 | В | If INV is low, B is an inverting receiver input and an inverting driver output. If INV is high, B is a noninverting receiver input and a noninverting driver output. |

Pin Description (continued)

| PIN | | NAME | FUNCTION |
|-----------|-----------|---------|---|
| MAX13450E | MAX13451E | NAME | FUNCTION |
| 10 | _ | Y | Noninverting Driver Output |
| 11 | 11 | GND | Ground |
| 12 | _ | Z | Inverting Driver Output |
| 13 | 13 | TERM100 | Termination Resistor Value Selection Input. Drive TERM100 low to select a 120Ω termination and high to select a 100Ω termination. The TERM100 input is referenced to V _L . |
| 14 | 14 | SRL | Slew-Rate Limiting-Enable Input. Drive SRL high to enable slew-rate limiting and low to disable slew-rate limiting. The SRL input is referenced to V _L . |
| _ | 8 | INV | Inversion Input. Drive INV high to internally swap RO logic level with respect to A and B signals. |
| _ | 9 | FAULT | Fault Flag Output. FAULT asserts high in overcurrent conditions or if A/B are forced below GND or above V _{CC} when the driver is enabled. FAULT is referenced to V _L . |
| _ | _ | EP | Exposed Pad |

Function Tables

Table 1. Termination Resistor Control (MAX13450E/MAX13451E)

| TERM | DE | RE | TERMINATION RESISTOR |
|------|---------|----|----------------------|
| Low | Χ | X | Activated |
| High | igh X X | | Not activated |

Table 2. Shutdown Control (MAX13450E/MAX13451E)

| DE | DE RE | | STATE |
|-----|-------|------|----------|
| Low | High | High | Shutdown |

Table 3. Function Table for Transmitter (MAX13450E)

| INF | PUT | OUTPUT | | | |
|--------|------|--------|--------|--|--|
| DE | DI | Υ | Z | | |
| Low | X | High-Z | High-Z | | |
| High | Low | Low | High | | |
| riigii | High | High | Low | | |

Table 4. Function Table for Receiver (MAX13450E)

| INPUT | | OUTPUT | |
|-------|-----------------|--------|--|
| RE | A-B | RO | |
| High | X | High-Z | |
| Low | ≥ -50mV or Open | High | |
| Low | ≤ -200mV | Low | |

Table 5. INV Input Function Table for Transmitter (MAX13451E)

| | INPUT | | OUTPUT | |
|------|-------|------|--------|--------|
| DE | INV | DI | Α | В |
| Low | Х | Х | High-Z | High-Z |
| | Low | Low | Low | High |
| High | | High | High | Low |
| High | High | Low | High | Low |
| | | High | Low | High |

Function Tables (continued)

Table 6. INV Input Function Table for Receiver (MAX13451E)

| INPUT | | | OUTPUT |
|-------|------|-----------------------------|--------|
| RE | INV | A-B | RO |
| High | X | X | High-Z |
| | Low | ≥ -50mV or Short or Open | High |
| Low | | ≤ -200mV | Low |
| LOW | High | ≥ -50mV or Open | Low |
| | | ≤ -200mV | High |

Detailed Description

The MAX13450E is a full-duplex, RS-485/RS-422-compatible transceiver and the MAX13451E is a half-duplex, RS-485/RS-422-compatible transceiver. Both devices have an internal $100\Omega/120\Omega$ termination resistor. The MAX13450E/MAX13451E have a VL supply voltage input to support down to a +1.8V voltage logic interface.

The MAX13450E/MAX13451E feature a 1/8-unit load receiver input impedance, allowing up to 256 transceivers on the bus. All line interface pins are protected to ±30kV ESD based on the HBM. These devices also include fail-safe circuitry, guaranteeing a defined logic-level receiver output when the receiver inputs are open or shorted.

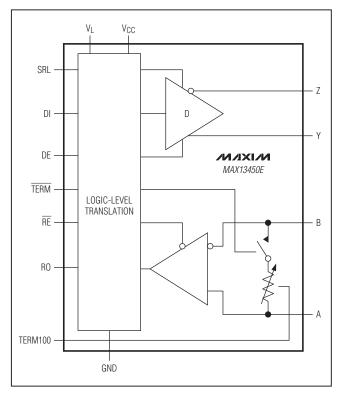
The MAX13450E/MAX13451E allow slew-rate-limited driver outputs for lower data rates below 500kbps. The SRL reduces the slew rate, which reduces EMI emissions and reflections caused by improperly terminated cables.

The MAX13451E has a FAULT output that indicates a fault condition on the driver. The MAX13451E also has an INV input that inverts the phase of A and B pins.

Termination Resistor

The MAX13450E/MAX13451E feature a selectable internal termination resistor. Drive the TERM input low to enable the internal termination resistor. Drive the TERM input high to disable the internal termination resistor.

_Functional Diagram (MAX13450E)



Drive the TERM100 input high to select the 100Ω termination resistor. Drive TERM100 input low to select the 120Ω termination resistor.

INV Input (MAX13451E)

The INV input of the MAX13451E reverses the polarity of the RO receiver output (see Table 5 and 6). If the INV input is high then the RO output is low under fail-safe receiver conditions. This is the opposite polarity of normal fail-safe operations.

Fault Condition (MAX13451E)

The MAX13451E also has a FAULT output to indicate a fault condition. The FAULT output is active high when there is a short circuit at the driver's output, an over/undervoltage at the driver's outputs, or the device's temperature is higher than +150°C.

Thermal Shutdown

When the devices' temperature goes over +150°C, the termination resistor turns off, and the transmitter shuts down while the receiver stays active.

Fail Safe

The MAX13450E guarantee a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver input threshold between -50mV and -200mV. If the differential receiver input voltage (A - B) is greater than or equal to -50mV, RO is logic-high. If (A - B) is less than or equal to -200mV, RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination resistor. With the receiver thresholds of the MAX13450E, this results in RO being logic-high.

The MAX13451E has the same fail-safe receiver behavior as the MAX13450E when the INV input is low. When the INV input is high, RO is low under the fail-safe condition.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the MAX13450E/MAX13451E have extra protection against static electricity. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX13450E/MAX13451E keep working without latchup or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX13450E/MAX13451E are characterized for protection to the following limits:

- ±30kV using the Human Body Model
- ±15kV using the Air Gap Discharge Method specified in IEC 61000-4-2
- ±7kV using the Contact Discharge Method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 11a shows the Human Body Model, and Figure 11b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a $1.5 \mathrm{k}\Omega$ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX13450E/MAX13451E help equipment designs to meet IEC 61000-4-2, without the need for additional ESD-protection components. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 11c shows the IEC 61000-4-2 model, and Figure 11d shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

Applications Information

Typical Applications

The MAX13450E transceiver is designed for full-duplex, bidirectional data communications on point-to-point or multipoint bus transmission lines (Figure 12). The MAX13451E transceiver is designed for half-duplex, bidirectional data communications on point-to-point or multipoint bus transmission lines (Figure 13).

256 Transceivers on the Bus

The standard RS-485 receiver input impedance is oneunit load, and the standard driver can drive up to 32-unit loads. The MAX13450E/MAX13451E have a 1/8-unit load receiver input impedance, allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of these devices, as well as other RS-485 transceivers with a total of 32-unit loads or fewer, can be connected to the line.

Reduced EMI and Reflections

The MAX13450E/MAX13451E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 500kbps.

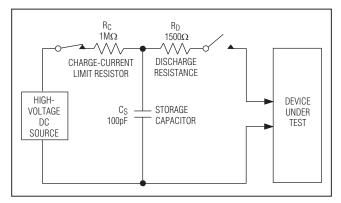


Figure 11a. Human Body ESD Test Model

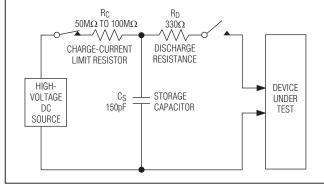


Figure 11c. IEC 61000-4-2 ESD Test Model

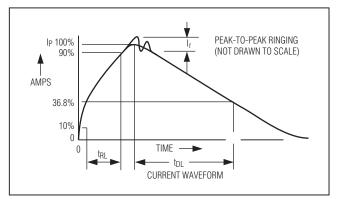


Figure 11b. Human Body Current Waveform

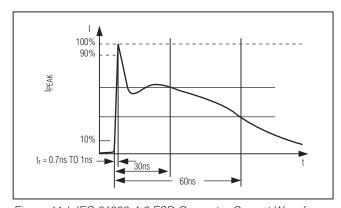


Figure 11d. IEC 61000-4-2 ESD Generator Current Waveform

Typical Application Circuits

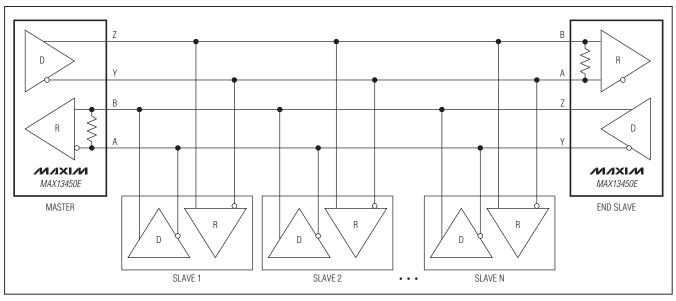


Figure 12. Full-Duplex, Multidrop (MAX13450E)

Typical Application Circuits (continued)

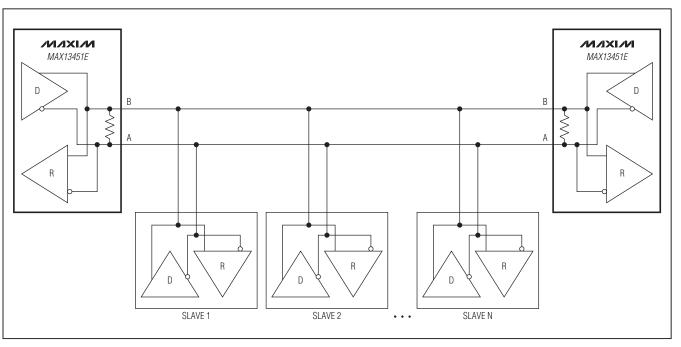


Figure 13. Half-Duplex, Multidrop, and Point-to-Point Systems (MAX13451E)

Low-Power Shutdown Mode

Drive $\overline{\text{RE}}$ high, DE low, and $\overline{\text{TERM}}$ high to enter low-power shutdown mode (see Table 2).

____Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. | |
|--------------|--------------|----------------|--|
| 14 TSSOP-EP | U14E+3 | <u>21-0108</u> | |

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|--------------------|---------------|-----------------|------------------|
| 0 | 4/10 | Initial release | _ |

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